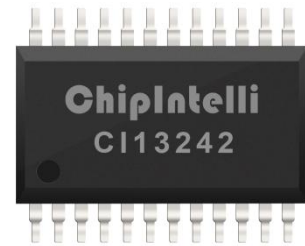


CI13242 Datasheet

High Cost Performance Automatic Speech Recognition Chip



- **Brain Neural Network Processing Unit (BNPU)**
 - BNPU V3.5 support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, call noise reduction
- **CPU and Storage**
 - CPU frequency up to 210 MHz
 - 2 MBytes of Flash memory inside
 - 288 KBytes of SRAM inside
 - 256 bit eFuse for encryption
- **Audio Codec**
 - High performance, Low-power consumption audio ADC with $\text{SNR} \geq 95\text{dB}$
 - Low-power consumption audio DAC with $\text{SNR} \geq 95\text{dB}$
- **PWM**
 - Four PWM interfaces
- **GPIO**
 - 13 fast GPIOs, response speed up to 20MHz
 - 7 GPIOs with 5V input tolerant capability
- **Reset and power management**
 - Build-in PMU
 - PMU input voltage range: 3.6V to 5.5V
 - Power-on Reset (POR)
 - Power Voltage Detector (PVD)
- **Clock management**
 - Built in RC oscillator
 - Support external crystal oscillator input
- **Communication interface**
 - One IIC interface
 - Three UART interfaces with 5V input tolerant capability , with 3Mbps baud rate
- **Timer and Watch dog**
 - Two 32-bit timers, One watch dogs

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1 Description

1.1 Functional overview

CI13242 is a high-performance artificial intelligence chip for speech recognition and processing. CI13242 integrates brain neural network processor BNPU V3.5 developed by chipintelli, 210Mhz CPU, up to 288 KByte SRAM, integrated PMU, integrated RC oscillator, integrated single channel high-performance low-power consumption audio codec, integrated multiple UART, IIC, PWM, GPIO and other peripheral control interfaces, only need a few peripheral device for internal LDO. It has high cost performance.

CI13242 uses industrial design standards and has high environmental reliability. The working temperature range of the chip is between - 40°C and + 85°C. It complies with MSL3 humidity sensitivity level, 4KV contact discharge test standard of IEC 61000-4-2, ROHS and REACH environmental protection standards.

CI13242 adopt the new generation BNPU technology of Chipintelli, which can support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, call noise reduction. It also support Chinese, English, Japanese and other global languages. can be widely used by home appliances, lighting, toys, wearable devices, industry, automobile and other product fields to realize voice interaction and control, and the application of various intelligent voice solutions It can implement the requirements of improving efficiency and reducing cost for the existing intelligent speech off-line recognition application.

1.2 Chip Specifications

The functional block diagram of CI13242 chip is shown in the figure below:

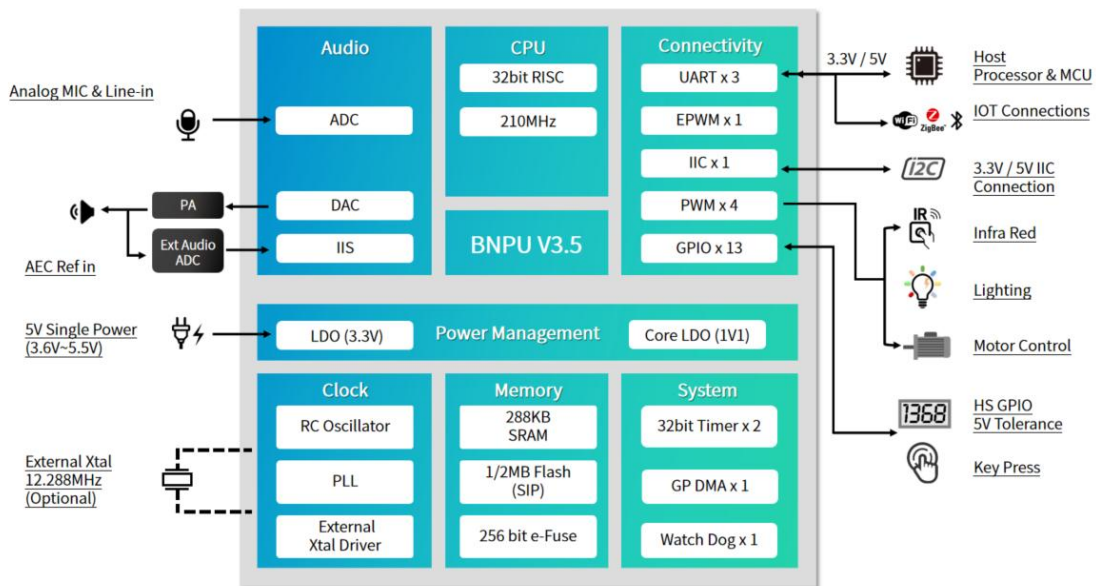


Figure 1-1 CI13242 Function Block Diagram

■ Brain Neural Network Processing Unit (BNPU) V3.5

- BNPU V3.5 support DNN \ TDNN \ RNN \ CNN and other neural networks and parallel vector operations. It can realize speech recognition, call noise reduction

■ CPU

- 32 bit high performance CPU, frequency up to 210 MHz

■ Storage

- 288KB SRAM inside
- 256bit e-Fuse inside
- 2MB Flash inside

■ Audio Interface

- High performance, Low consumption audio codec module, support single ADC sampling and signal DAC playing
- Support automatic level control (ALC)
- Support 8kHz/16kHz/24kHz/32kHz/44.1kHz/48kHz Sampling rate

■ PMU

- Supports wide power supply voltage, with a power supply range of 3.6V to 5.5V
- Built in 2 high-performance LDO circuits, no need to configure external power chips, application solutions only require a small number of peripheral resistive and capacitive devices

■ CLOCK

- Built in RC oscillator
- Support external crystal oscillator input

■ Peripheral Interface and Timer

- Three UART interfaces with 3M baud rate maximum
- One IIC interface, support IIC extended device
- Four PWM interfaces, support direct driving for light control and motor applications
- Two 32-bit timers inside
- Built-in one independent watchdog (IWDG)

■ GPIO

- Support 13 GPIOs, Can be used as the main control IC application
- 7 GPIOs with 5V tolerant capability. There is no need for external 5V conversion, but the external resistance needs to be pulled up to 5V
- Each GPIO can be configurable for interruption and support pull up and pull down setting

■ Development Support

- Provide software development package, application examples and notices
- Content and services can be realized online, obtain address:

<https://aiplatform.chipintelli.com>

■ Firmware burning and protection

- Support firmware upgrade by UART and firmware protection

■ ESD

- Excellent ESD design, it can pass 4KV contact discharge test

■ ROHS and REACH

- Support ROHS and REACH standards

■ Packaging and Operating temperature

- Devices Packaging: SSOP24, Length*Width*Thickness = 8.6*6.0*1.64 mm
- Operating temperature: -40°C~+85°C

2 Pin Diagram and Function Description

2.1 Pin Diagram

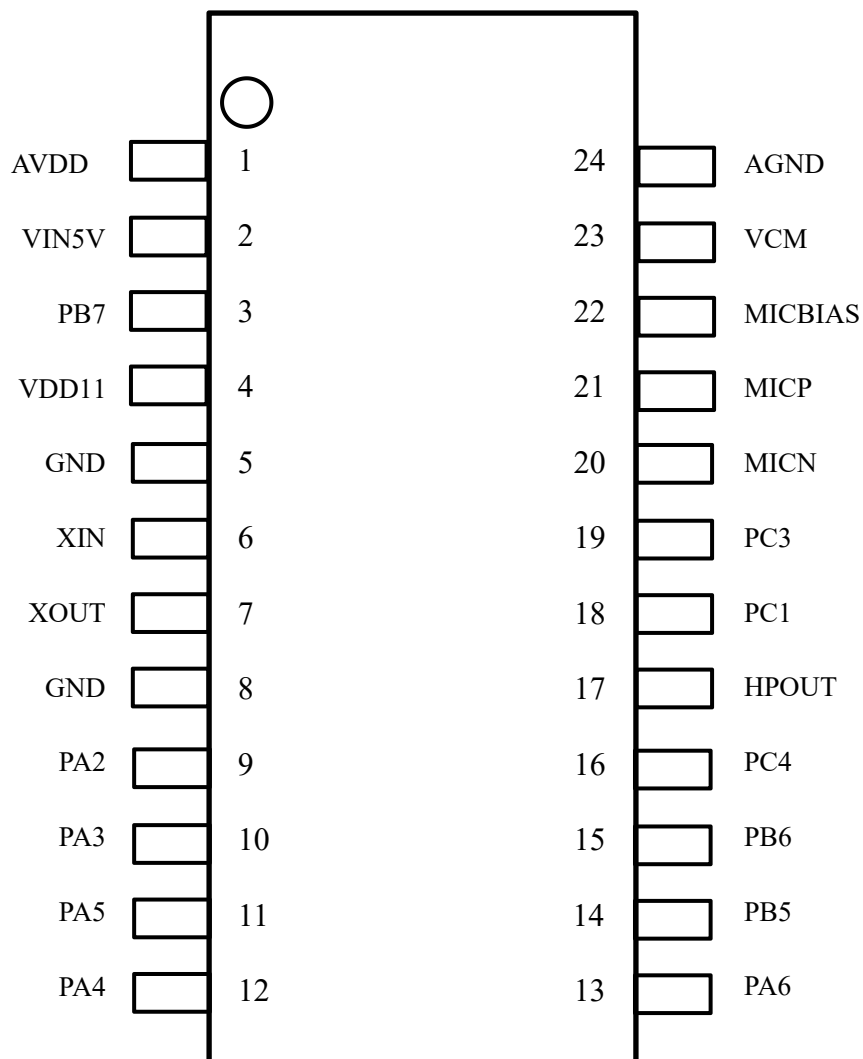


Figure 2-1 CI13242 Pin Sequence and Definition Diagram

2.2 Pin descriptions

Table 2-1 Pin Descriptions

Pin number	Pin Name	Type	IO 5V withstand voltage	IO power on default state	Pin reuse and functional description

1	AVDD	P	-	-	<ul style="list-style-type: none"> ● Internal LDO-3.3V output ● Internal analog circuit 3.3V power supply input ● * Note1*
2	VIN5V	P	-	-	<ul style="list-style-type: none"> ● Power supply voltage range 3.6V to 5.5V ● * Note1*
3	PB7	IO	-	IN, T+U	<ul style="list-style-type: none"> ● GPIO PB7
4	VDD11	P	-	-	<ul style="list-style-type: none"> ● LDO-1.1V output ● Core 1.1V power input ● * Note1*
5	GND	P	-	-	Ground
6	XIN	I	-	-	<ul style="list-style-type: none"> ● XIN ((Initial state at startup) ● GPIO PA0 ● PWM2
7	XOUT	O	-	-	<ul style="list-style-type: none"> ● XOUT ((Initial state at startup) ● GPIO PA1
8	GND	P	-	-	Ground
9	PA2	IO	√	IN, T+D	<ul style="list-style-type: none"> ● GPIO PA2 ((Initial state at startup) ● IIS SDI ● IIC SDA ● UART1 TX ● PWM0 ● PEMP
10	PA3	IO	√	IN, T+D	<ul style="list-style-type: none"> ● GPIO PA3 ((Initial state at startup) ● IIS_LRCLK ● IIC_SCL ● UART1_RX1 ● PWM1 ● PEMN
11	PA5	IO	√	IN, T+D	<ul style="list-style-type: none"> ● GPIO PA5 ((Initial state at startup) ● IIS_SCLK ● - ● UART2_TX ● PWM3 ● PWMN
12	PA4	IO	√	IN, T+U	<ul style="list-style-type: none"> ● GPIO PA4 ((Initial state at startup) /PG_EN (When powered on, the programming function is activated during high battery life) ● IIS_SDO ● - ● - ● PWM2 ● PWMP
13	PA6	IO	√	IN, T+D	<ul style="list-style-type: none"> ● GPIO PA6 ((Initial state at startup) ● IIS_MCLK ● - ● UART2_RX ● PWM0
14	PB5	IO	√	IN, T+U	<ul style="list-style-type: none"> ● GPIO PB5 ((Initial state at startup) ● UART0_TX ● IIC_SDA ● PWM1 ● PWMP
15	PB6	IO	√	IN, T+U	<ul style="list-style-type: none"> ● GPIO PB6 ((Initial state at startup) ● UART0_RX

					<ul style="list-style-type: none"> ● IIC_SCL ● PWM2 ● PWMN
16	PC4	IO	-	IN, T+U	<ul style="list-style-type: none"> ● Reserve ((Initial state at startup)) ● GPIO PC4 ● SCL ● PWM0
17	HPOUT	O	-	-	DAC output
18	PC1	IO	-	IN, T+D	<ul style="list-style-type: none"> ● Reserve ((Initial state at startup)) ● GPIO PC1 ● 3.TX2 ● PWM3
19	PC3	IO	-	IN, T+D	<ul style="list-style-type: none"> ● Reserve ((Initial state at startup)) ● GPIO PC3 ● SDA ● PWM1
20	MICN	I	-	-	Microphone N input
21	MICP	I	-	-	Microphone P input
22	MICBIAS	O	-	-	Microphone bias output
23	VCM	O	-	-	VCM Output
24	AGND	P	-	-	Analog ground

* Note1* The pins need to be externally connected to a 4.7uF capacitor

* Note2* When powered on, the pin is at a high level, and the system will enter programming mode

Conformity with definition:

I input

O output

IO bidirectional

P power or ground

T+D Tristate plus pull-down

T+U Tristate plus pull-up

OUT power-on defaults to output mode

IN power-on defaults to input mode

All IO supports driver capabilities that can be matched, and up and down resistors that can be matched.

2.3 Alternate functions

Table 2-2 IO Alternate Functions

Pin Name	Function1	Function2	Function3	Function4	Function5	Function6	Specific Function
XIN	PA0	PWM2					XIN
XOUT	PA1						XOUT
PA2	PA2	SDI	IIC_SDA	UART1_TX	PWM0	PWMP	
PA3	PA3	LRCK	IIC_SCL	UART1_RX	PWM1	PWMN	
PA4	PA4	SDO	-	-	PWM2	PWMP	PG EN Note1
PA5	PA5	SCLK		TX2	PWM3	PWMN	
PA6	PA6	MCLK		RX2	PWM0		
PB5	PB5	UART0_TX	IIC_SDA	PWM1	PWMP		
PB6	PB6	UART0_RX	IIC_SCL	PWM2	PWMN		
PC4	-	PC4	SCL	PWM0			
PC1	-	PC1	TX2	PWM3			
PC3	-	PC3	SDA	PWM1			

Note1: The PA4 (PG-EN) pin is pulled up by default internally. When the system detects that the pin is at a high level and there is a firmware upgrade signal on the UART0 interface when powered on, it automatically enters the upgrade mode. At this time, the internal Flash of the chip can be programmed using the upgrade tool. If the system does not detect a firmware upgrade signal on the UART0 interface or detects a low voltage on the PA4 pin at this time, it will enter normal working mode.

3 Electrical Characteristics

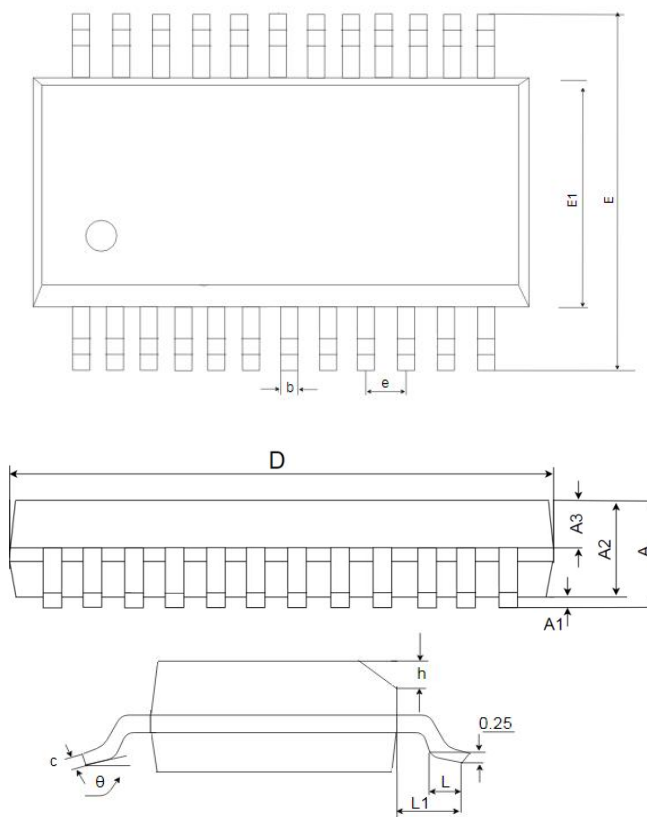
Table 3-1 Electrical Characteristics Table

Symbol	Description	Min.	Typical	Max.	Unit
VIN5V	Chip power supply *Note1*	3.6	5.0	5.5	V
AVDD	3.3V power	2.97	3.3	3.63	V
VDD11	1.1V power	0.99	1.1	1.21	V
V _{IH}	Input High Voltage ($3.0V \leq VDD33 \leq 3.6V$)	$0.7 \times VDD33$	-	$VDD33 + 0.3$	V
V _{IL}	Input Low Voltage ($3.0V \leq VDD33 \leq 3.6V$)	-0.3	-	$0.3 \times VDD33$	V
V _{OL}	Output Low Voltage @I _{OL} = 12mA	-	-	0.4	V
V _{OH}	Output High Voltage @I _{OH} = 20mA	2.4	-	-	V
I5V-IO	Driving current when IO (withstand 5V voltage) outputs 3.3V	20	-	33	mA
I3V3-IO	Driving current when IO (withstand 3.3V voltage) outputs 3.3V	14	-	24	mA
ΣIVDD	Driving current of all IO	-	-	260	mA
P _{de}	5V power supply, and the chip's VDD11 is powered by external DC-DC chip. The total power consumption of 5V input during normal identification at TA= 25°C	40	-	90	mW
P _{di}	5V power supply, and the chip uses internal PMU. The total power consumption of 5V input during normal identification at TA= 25°C	125	-	255	mW
RC Oscillator Accuracy *Note2*	TA: -40°C~+85°C	-1.5	-	+1.5	%
Top	Chip working environment temperature	-40	-	+85	°C
Tst	Chip storage environment temperature	-55	-	+150	°C

Note1: Require ripple to be less than 300mVp-p.

Note2: Due to the principles and characteristics of semiconductor technology, the built-in RC oscillator of the chip will produce a certain temperature drift ($\pm 1.5\%$) in its oscillation frequency accuracy in high and low temperature environments. CI13242 has a built-in baud rate adaptive circuit, which can support normal communication between the chip and the upper computer in high and low temperature environments. If the application plan requires the clock of the chip to be very accurate, please use a chip equipped with an external crystal oscillator and corresponding application plan from chipintelli.

4 Packaging Information



COMMON DIMENSIONS

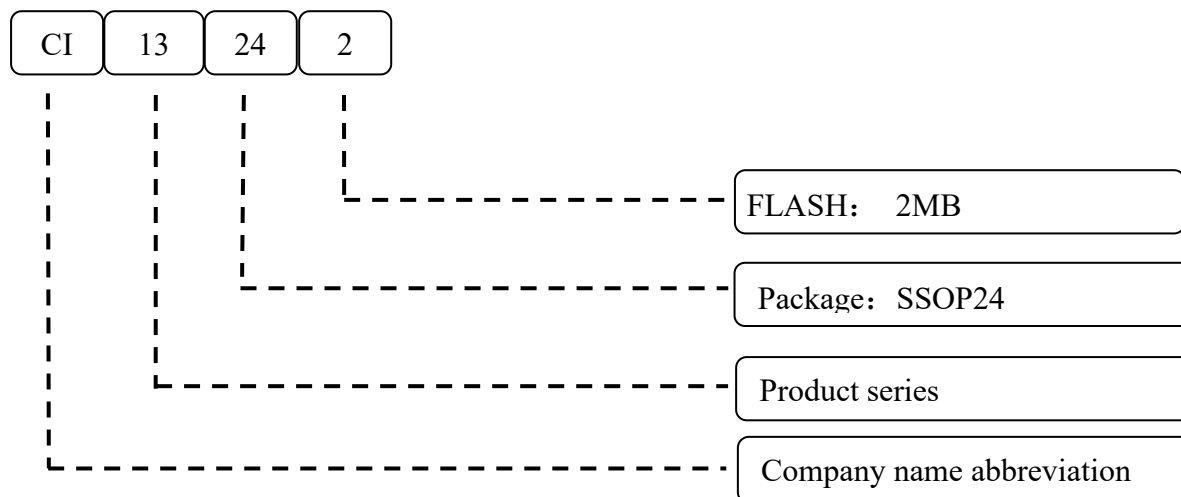
SYMBOL	UNIT: MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.15	0.25
A2	1.30	1.48	1.50
A3	0.6	0.65	0.70
b	0.23	—	0.31
c	0.20	—	0.24
D	8.55	8.6	8.75
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	0.635BSC		
h	0.30	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

5 Order Information

The MRAK for CI13242 chip packaging is shown in the following figure. The first line is the company logo, the second line is the chip model, and the third line is the production batch number. The dot in the bottom left corner is the 1-pin identifier.



The definition of chip model is as follows:



The ordering information of CI13242 chip is shown in Table 5-1.

Table 5-1 Order Information Table

Orderable Device	Flash	Status	Package Type	Pins	Package Qty	Eco Plan	MSL Peak Temp	Op Temp (°C)
CI13242	2MByte	MP	SSOP24/Tube	24	50	RoHS & Green	Level-3 260C-UNLIM	-40 to 85

6 Application

6.1 Application Reference Circuit Diagram

The CI13242 chip only requires a small amount of peripheral components to support various voice applications. For the voice part, the chip can support single microphone differential input or single microphone single ended input. Users can choose the appropriate circuit based on the designed application scheme's functionality, power consumption, and cost requirements. Below is a specific description of the simplest application reference circuit diagram for this chip.

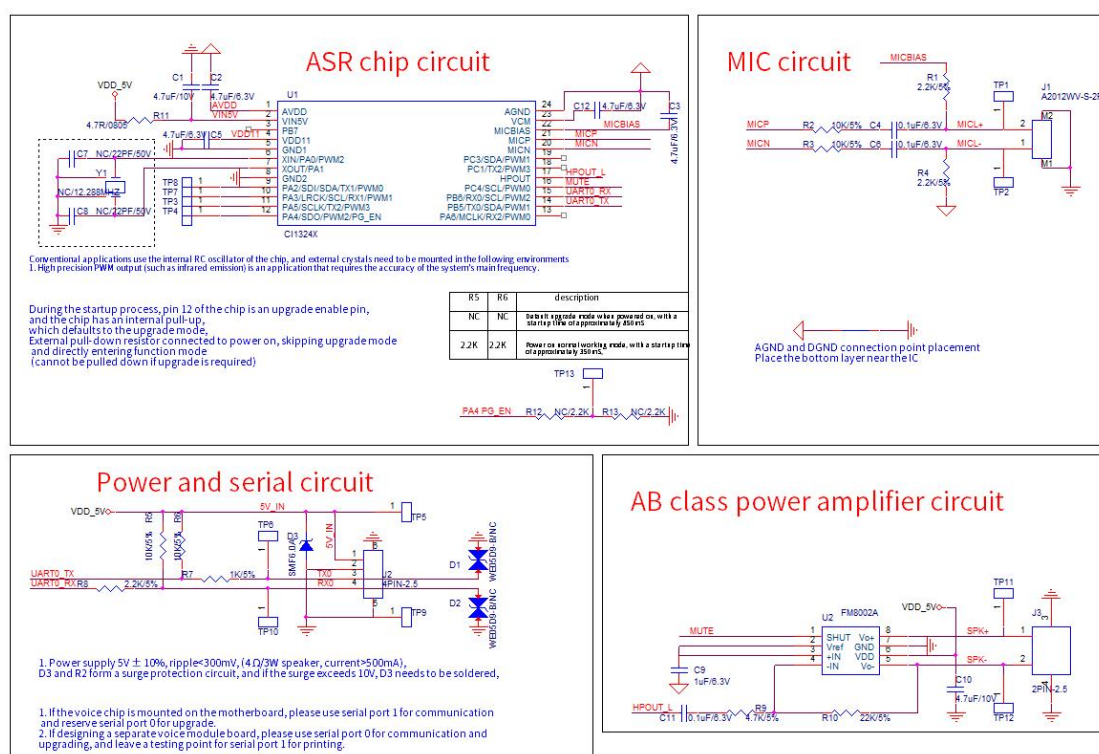


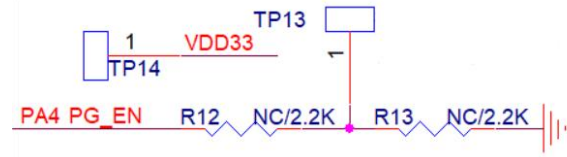
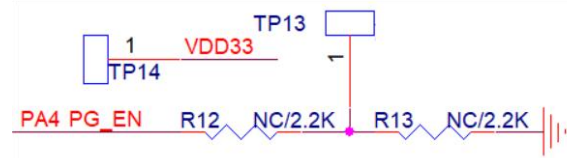
Figure 6-1 The circuit diagram of the simplest CI13242's application scheme

The above diagram shows a typical application scenario for the differential input and amplifier output of a single microphone in the CI1324X series chip, including CI13242. Users can design according to the corresponding peripheral device specifications in the diagram.

When designing the schematic, if the board level online upgrade function needs to be considered, the UART0 pin can be led out to facilitate the firmware upgrade of the flash inside the main chip through UART0 after the PCB board is mounted. The PA4 (PG-EN) pin of the chip has an internal pull-up function, and when powered on, it defaults to the upgrade mode. After turning on, the upgrade signal from the external UART0 port should be detected, and if there is one, the upgrade should be initiated directly. The default startup time of the chip has been extended due to the addition of upgrade mode detection, approximately 850ms; If users have high requirements for startup time, they can lead out the PA4 pin, add two 2.2K Ω pull-down resistors to the ground, and

add a test point between the two 2.2K Ω resistors. At this time, the chip will start up in normal mode, with a startup time of about 350mS, which can shorten the startup time. If you want to upgrade online at this time, you can supply a high level to the middle test point connected by two 2.2K Ω resistors externally, pull the PA4 pin high, and then upgrade through UART0.

Table 6-1 CI1324X Upgrade Mode Table

PG_EN External Resistance Diagram	R5\R6 Installation	PG_EN High and low levels	Turn on Time
	R5\R6 NC	High level, upgrade mode	850ms
	R5\R6 sticker 2.2K	Low level, working mode	350ms

The chip solution can choose either a differential microphone design or a single ended microphone design. It is recommended to use the differential microphone design shown in the above figure. If the user has cost requirements, the microphone part in the above figure can be modified to a single ended microphone design, which can use fewer passive components than differential microphones. However, this method is only recommended for use in situations where the microphone line length is less than 20 centimeters. Otherwise, due to the long line, the anti-interference effect may not be sufficient, resulting in better speech recognition than differential microphone design. The amplifier in the above diagram uses Class AB power amplifiers, and it is recommended to use the 8002 power amplifier chip. Users can also choose the power amplifier chip according to the requirements of the plan. If the power amplifier function is not needed, this part of the circuit can also be removed to reduce costs.

If users do not have special requirements for the power consumption of the solution, it is recommended to directly use the internal PMU power supply of the chip. If there is a power consumption requirement, an external DCDC chip can be added to supply 1.1V power to the chip to reduce power consumption. The UART ports of the chip all support 5V communication. The UART0 port in the above figure is connected to a 3.3V signal. If you want to connect 5V, you can add pull-up resistors connected to 5V around the RX and TX pins of UART0, without the need for additional voltage conversion circuits.

6.2 Other Application Notices

1. The built-in RC oscillator of the chip will produce a certain temperature drift ($\pm 1.5\%$) in high and low temperature environments due to semiconductor technology principles. The chip is equipped with baud rate adaptive hardware, which can adapt to normal communication with the upper computer in different temperature environments when turned on. If the application requires higher clock accuracy, please use the CI1324X series chip and use an external crystal oscillator.
2. The chip integrates a PMU management unit, which includes two LDOs that provide 3.3V and 1.1V voltages to the chip, respectively. If there are no special requirements for power consumption, the solution does not require an external power chip, and the ripple of the external 5V power supply must be less than 300mV.
3. CI13242 is made of lead-free environmentally friendly materials. When SMT welding, please set the furnace temperature and time parameters according to lead-free standards. As shown in the following figure

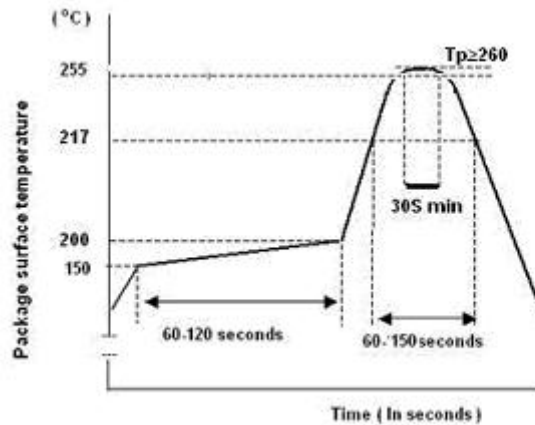


Figure 6-2 Furnace Temperature Curve

4. The use, handling, production and processing of CI13242 require attention to anti-static measures, and its packaging should use anti-static materials.

- Chipintelli reserves the right to change the instruction without further notice. Customers should obtain the latest version before placing an order, and verify that the relevant information is complete and up-to-date.
- Under specific conditions, any semiconductor product has a certain possibility of failure or failure. The buyer has the responsibility to comply with safety standards and take safety measures when using the product for system design and manufacturing, to avoid potential failure risk which may cause personal injury or property loss.
- Product improvement is endless. Chipintelli will provide customers with better products wholeheartedly!